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APPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/626,775	07/25/2003	Hee Bok Kang	40296-0030	1859		
26633 7	26633 7590 11/02/2004			EXAMINER		
	RMAN WHITE & M	NGUYEN, VAN THU T				
1666 K STREI SUITE 300	21,NW	ART UNIT	PAPER NUMBER			
WASHINGTON, DC 20006			2824			

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Applic	cation No.	Applicant(s)				
		10/62	6,775	KANG, HEE BOK				
	Office Action Summary	Exam	iner	Art Unit				
			u Nguyen	2824				
Period fo	The MAILING DATE of this communor Reply	nication appears on	the cover sheet with the c	correspondence ad	ldress			
THE - Exte after - If the - If NC - Failt Any	ORTENED STATUTORY PERIOD F MAILING DATE OF THIS COMMUN nsions of time may be available under the provisions SIX (6) MONTHS from the mailing date of this come period for reply specified above is less than thirty (3) period for reply is specified above, the maximum si re to reply within the set or extended period for reply reply received by the Office later than three months ed patent term adjustment. See 37 CFR 1.704(b).	IICATION. s of 37 CFR 1.136(a). In n nunication. 30) idays, a reply within the tautory period will apply a y will, by statute, cause the	o event, however, may a reply be tin statutory minimum of thirty (30) day nd will expire SIX (6) MONTHS from application to become ABANDONE	nely filed s will be considered timel the mailing date of this or D (35 U.S.C. § 133).				
Status								
1)[\]	Responsive to communication(s) file	ed on <i>17 Septemb</i>	er 2004					
2a)□		2b)⊠ This action						
3)		•		secution as to the	e merits is			
٠,۵	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disposit	ion of Claims							
4)⊠ 5)□ 6)⊠ 7)□	Claim(s) 1-20 is/are pending in the application.  4a) Of the above claim(s) 11-18 is/are withdrawn from consideration.  Claim(s) is/are allowed.  Claim(s) 1-10, 19-20 is/are rejected.							
Applicat	ion Papers							
9)☐ The specification is objected to by the Examiner.								
10)🛛	10)⊠ The drawing(s) filed on <u>25 July 2003</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.							
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11)	11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority (	ınder 35 U.S.C. § 119							
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>								
Attachmen	t(s)							
	e of References Cited (PTO-892)		4) Interview Summary					
3) 🔯 Inforr	e of Draftsperson's Patent Drawing Review (F nation Disclosure Statement(s) (PTO-1449 or r No(s)/Mail Date <u>07/25/2003</u> .		Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:		)-152)			

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### **DETAILED ACTION**

#### Election/Restrictions

- 1. Claims 11-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Groups II-IV, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on September 17, 2004. Applicant is required to cancel claims 11-18 in the next response.
- 2. Claims 1-10, 19-20 are present for examination.

# Claim Rejections - 35 USC § 112

- 3. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.
- FIG. 7 shows a register controller 510 comprising a register array 511 and a register command processor 512. However, there is no drawing shows a register controller comprising a nonvolatile memory unit, a register array, and a register command processor as claimed in claim 2.

# Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

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international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Keays (U.S. Patent No. 6,614,695).

Regarding claim 1, Keays disclose, in FIG. 1, a memory device (100) capable of controlling a characteristic parameter, comprising:

a nonvolatile memory unit (104) for storing data in the nonvolatile memory unit; a register controller (108 and 130); and

a parameter controller (112/114/116) configured to output a signal having a characteristic parameter depending on a signal outputted from the register controller.

(See column 5, line 14 to column 6, line 5)

Regarding claim 2, Keays further disclose the register controller comprises a register array (130) comprising a plurality of registers (130(a)-130(d)); and a register command processor (108) configured to receive a plurality of signals (from Processor 131, see FIG. 2), to identify a mode as a program mode or a read mode by decoding the plurality of signals, and individually control the plurality of registers according to the identified mode.

Regarding claim 19, it is rejected under U.S.C. 102(e) since it recited similar limitations as in claim 1.

6. Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by Merritt et al. (U.S. Patent No. 6,484,278).

Regarding claim 19, Merritt et al. discloses, in FIG. 4, an integrated circuit device capable of receiving an input signal and generating an output signal having signal performance characteristics comprising a signal performance characteristic controller (302) configured to

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control one or more of the signal performance characteristics (DQ) of the integrated circuit device.

### Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keays and Komatsuzaki (PGPUB. 2004/0047172).

Keays discloses, as applied in prior rejection of claim 1, all claimed subject matter except further limitations as in claims 9-10.

Komatsuzaki discloses, in FIG. 12, a ferroelectric memory device comprising:

a plurality of unit cells;

a plurality of switches (for each unit cells); and

bit lines comprising sub bit lines connected to the plurality of unit cells and a main bit line connected to the plurality of sub bit lines via the plurality of switches,

wherein the plurality of switches is configured so that when a predetermined unit cell of the plurality of unit cells is accessed, only a switch for connecting a particular one of the plurality of sub bit lines connecting the predetermined unit cell to the main bit line is turned on, and other switches for connecting the rest of the plurality of sub bit lines to the main bit line are all turned off (corresponding to selected word line and sub bit line).

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Since Keays and Komatsuzaki are both from the same field of endeavor, the purpose disclosed by Komatsuzaki would have been recognized in the pertinent art of Keays.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace the flash memory in Keays with the FeRAM in Komatsuzaki because FeRAM is also an applicable non-volatile memory type.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Merritt et al.

Regarding claim 20, Merritt et al. further discloses, in FIG. 4, the signal performance characteristic controller comprises:

a register controller (303) configured to provide a plurality of control signals (/RESET, ENABLE, SHIFT, /SHIFT);

a plurality of registers (R1-RN) each coupled to the register controller to receive as an input at least one of the plurality of control signals and configured to generate, in response to the at least one control signal, a register output signal as an output (ERROR1-ERRORN); and

a plurality of transistors (T1-TN) each comprising a drain coupled to a voltage source (Ground), a gate configured to receive the register output signal of at least one of the plurality of registers, and a source, wherein each of the sources of two or more of the plurality of transistors are coupled to a common output, wherein the common output controls the signal performance characteristic of the integrated circuit device (see FIG. 5).

Even though Merritt et al. have interchanged the circuit connection of the sources and drains of the plurality of transistors with respect to claimed limitation, it would have been

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obvious to one with ordinary skill in the art to realize that source and drain terminals of a transistor are interchangeable in a circuit performance.

## Allowable Subject Matter

10. Claims 3-8 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

### Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 29, 2004

VanThu Nguyen **Primary Examiner** Art Unit 2824